

IN THE CLAIMS:

*Kindly cancel non-elected claims 15-28 without prejudice or disclaimer.*

*Kindly replace claims 1, 2, and 4 with the following corresponding replacement claims:*

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--1. (Twice Amended) A semiconductor device exhibiting a high breakdown voltage, the semiconductor device comprising:

a first region of a first conductivity type;

a second region of a second conductivity type formed selectively in the surface portion of the first region;

*fig. 13*  
a third region of the first conductivity type formed selectively in the surface portion of the first region, the second region and the third region being spaced apart from each other;

a fourth region of the first conductivity type formed selectively in the surface portion of the second region;

*B*  
an offset region of the second conductivity type formed selectively in the surface portion of the first region between the second region and the third region;

a first insulation film on the offset region;

a gate electrode above the extended portion of the second region extending between the fourth region and the first region with a gate insulation film interposed between the extended portion of the second region and the gate electrode;

a first main electrode on the fourth region; and

a second main electrode on the third region;

wherein the offset region comprises a plurality of sub-regions aligned between the second region and the third region, the impurity concentrations of the sub-regions being different from each other, and.

wherein the offset region becomes a depletion layer when the device is turned OFF.--

--2. (Twice Amended) The semiconductor device according to Claim 1, wherein the depths of the sub-regions of the offset region are different from each other.--

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--4. (Twice Amended) A semiconductor device exhibiting a high breakdown voltage, the semiconductor device comprising:

a semiconductor substrate of a second conductivity type;

a first region of a first conductivity type formed selectively in the surface portion of the semiconductor substrate;

a second region of the second conductivity type formed selectively in the surface portion of the semiconductor substrate;

*fig. 15*  
a third region of the first conductivity type formed selectively in the surface portion of the first region;

the second region and the third region being spaced apart from each other;

*B<sup>2</sup>*  
a fourth region of the first conductivity type formed selectively in the surface portion of the second region;

an offset region of the second conductivity type formed selectively in the surface portion of the first region between the second region and the third region;

a first insulation film on the offset region;

a gate electrode above the extended portion of the second region extending between the fourth region and the first region with a gate insulation film interposed between the extended portion of the second region and the gate electrode;

a first main electrode on the fourth region; and

a second main electrode on the third region;

wherein the offset region comprises a plurality of sub-regions aligned between the second region and the third region, the impurity concentrations of the sub-regions being different from each other, and

wherein the offset region becomes a depletion layer when the device is turned OFF.--